

**Abstract of the Disclosure**

A thermal processing method is described which improves integrated circuit metal polishing and increases conductivity following polish. A method of fabricating a metal layer in an integrated circuit is described which comprises the steps of depositing a layer of metal alloy which contains alloy dopant precipitates, and performing a first anneal of the integrated circuit to drive the alloy dopants into solid solution. The metal is quenched to prevent the alloy dopants from coming out of solution prior to removing excess metal alloy with a polish process. To improve conductivity after polishing, the dopants are allowed to come out of solution. The metal alloy is described as aluminum with alloy dopants of silicon and copper where the first anneal is performed at 400 to 500° C. This process is particularly applicable to fabrication of interconnects formed using a dual damascene process. The integrated circuit is described as any circuit, but can be a memory device such as a DRAM.

"Express Mail" mailing label number: EL873859962US

Date of Deposit: August 30, 2001

This paper or fee is being deposited on the date indicated above with the United States Postal Service pursuant to 37 CFR 1.10, and is addressed to the Commissioner for Patents, Box Patent Application, Washington, D.C. 20231.